CLAIMS

What is Claimed is:

1. A semiconductor integrated circuit device including a digital circuit and an analog circuit which are integrated on a single semiconductor chip, said device comprising:

a first electrostatic destruction protection circuit, connected to the digital circuit, for protecting the digital circuit from destruction caused by ESD in the digital circuit by an influence of an input digital signal; and

a second electrostatic destruction protection circuit, connected to the analog circuit, for protecting the analog circuit from destruction caused by ESD in the analog circuit by an influence of an input analog signal,

wherein a first grounding conductor connected to the first electrostatic destruction protection circuit and a second grounding conductor connected to the second electrostatic destruction protection circuit are connected to each other outside the semiconductor integrated circuit device.

2. The semiconductor integrated circuit device of Claim 1, wherein

the first grounding conductor and the second grounding conductor are connected to each other inside a package substrate of the semiconductor integrated circuit device.

3. The semiconductor integrated circuit device of Claim 1, wherein

the first grounding conductor and the second grounding conductor are connected to each other outside a package substrate of the semiconductor integrated circuit device.

4. The semiconductor integrated circuit device of Claim 1, wherein

the first grounding conductor and the second grounding conductor are connected to each other using a capacitance outside a package substrate of the semiconductor integrated circuit device.

5. The semiconductor integrated circuit device of Claim 1, wherein

the first grounding conductor and the second grounding conductor are connected to

each other via a member for electrically connecting the semiconductor integrated circuit device to a package substrate of the semiconductor integrated circuit device.

6. A method for fabricating a semiconductor integrated circuit device including a digital circuit and an analog circuit which are integrated on a single semiconductor chip, said method comprising:

a circuit test step of judging whether or not the digital circuit connected to a first electrostatic destruction protection circuit for protecting the digital circuit from destruction caused by ESD in the digital circuit by an influence of an input digital signal and the analog circuit connected to a second electrostatic destruction protection circuit for protecting the analog circuit from destruction caused by ESD in the analog circuit by an influence of an input analog signal satisfy the specification;

an electrostatic destruction test step of, when it is judged in the circuit test step that both the digital circuit and the analog circuit satisfy the specification, judging whether or not destruction caused by ESD occurs for the digital circuit and the analog circuit; and

an external connection step of, when it is judged in the electrostatic destruction test step that destruction caused by ESD occurs in at least one of the digital circuit and the analog circuit, connecting a first grounding conductor connected to the first electrostatic destruction protection circuit to a second grounding conductor connected to the second electrostatic destruction protection circuit outside the semiconductor integrated circuit device.

7. The method for fabricating a semiconductor integrated circuit device of Claim 6, wherein

the external connection step is the step of connecting the first grounding conductor to the second grounding conductor inside a package substrate of the semiconductor integrated circuit device.

8. The method for fabricating a semiconductor integrated circuit device of Claim 6, wherein

the external connection step is the step of connecting the first grounding conductor to the second grounding conductor outside a package substrate of the semiconductor integrated circuit device.

9. The method for fabricating a semiconductor integrated circuit device of Claim 6, wherein

the external connection step is the step of connecting the first grounding conductor to the second grounding conductor using a capacitance outside a package substrate of the semiconductor integrated circuit device.

10. The method for fabricating a semiconductor integrated circuit device of Claim 6, wherein

the external connection step is the step of connecting the first grounding conductor to the second grounding conductor via a member for electrically connecting the semiconductor integrated circuit device to a package substrate of the semiconductor integrated circuit device.

11. A method for fabricating a semiconductor integrated circuit device, comprising:

a first package production step of producing a first package substrate in which a first grounding conductor connected to a first electrostatic destruction protection circuit for protecting a first digital circuit from destruction caused by ESD in the first digital circuit by an influence of an input digital signal and a second grounding conductor connected to a second electrostatic destruction protection circuit for protecting a first analog circuit from destruction caused by ESD in the first analog circuit by an influence of an input analog signal are not connected to each other inside a package substrate of a first semiconductor integrated circuit device including the first digital circuit and the first analog circuit which are integrated on a single semiconductor chip;

a second package production step of producing a second package substrate in which a third grounding conductor connected to a third electrostatic destruction protection circuit for protecting a second digital circuit from destruction caused by ESD in the second digital

circuit by an influence of an input digital signal and a fourth grounding conductor connected to a fourth electrostatic destruction protection circuit for protecting a second analog circuit from destruction caused by ESD in the second analog circuit by an influence of an input analog signal are connected to each other inside a package substrate of a second semiconductor integrated circuit device including the second digital circuit and the second analog circuit which are integrated on a single semiconductor chip;

a first LSI test step to be performed after the first package production step, including a first circuit test step of judging whether or not the first digital circuit and the first analog circuit satisfy the specification and a first electrostatic destruction test step of, when it is judged in the first circuit test step that both the first digital circuit and the first analog circuit satisfy the specification, judging whether or not destruction caused by ESD occurs for the first digital circuit and the first analog circuit;

a second LSI test step to be performed after the second package production step, including a second circuit test step of judging whether or not the second digital circuit and the second analog circuit satisfy the specification and a second electrostatic destruction test step of, when it is judged in the second circuit test step that both the second digital circuit and the second analog circuit satisfy the specification, judging whether or not destruction caused by ESD occurs for the second digital circuit and the second analog circuit;

a first package selection step of, when it is judged in the first electrostatic destruction test step of the first LSI test step that no destruction caused by ESD occurs in both the first digital circuit and the first analog circuit, selecting the first package substrate; and

a second package selection step of, when it is judged in the first electrostatic destruction test step of the first LSI test step that destruction caused by ESD occurs in at least one of the first digital circuit and the first analog circuit and it is judged in the second electrostatic destruction test step of the second LSI test step that no destruction caused by ESD occurs in both the second digital circuit and the second analog circuit, selecting the second package substrate.